



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
|-----------------|-------------|----------------------|---------------------|------------------|

09/556,779

04/25/2000

Seong-Hwan Moon

06192.0116

8043

7590

10/22/2004

McGuire Woods LLP
1750 Tysons Boulevard Suite 1800
McLean, VA 22102

EXAMINER

KUMAR, SRILAKSHMI K

ART UNIT

PAPER NUMBER

2675

DATE MAILED: 10/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/556,779

Applicant(s)

MOON ET AL.

Examiner

Srilakshmi K. Kumar

Art Unit

2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 June 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Art Unit: 2675

DETAILED ACTION

Response to Amendment

The following is in response to the Response sent on June 22, 2004. No claims have been amended.

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
4. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita et al (US 6,388,651) in view of Hashimoto (US 5,973,660) and further in view of Ikeda et al (US 6,222,518).

Art Unit: 2675

As to independent claim 1, Kinoshita et al disclose in Figs. 1-4, a liquid crystal display (1) comprising, a signal processor (Fig. 3, item G/A) for generating and outputting a first image signal and a second image signal (out of the left and right of G/A), a driving control signal using an image data (into 701b-708b)), a main control signal (into G/A), the driving control signal including a source driving control signal including a source driving control signal and a gate driving control signal (col. 1, line 64-col. 2, line 12);

and a power source all of which are supplied from an image supplying source; Kinoshita et al does not state a power source. It would have been obvious to one of ordinary skill in the art that a power source is present as it is required in order for the liquid crystal display to operate.

a data signal driver for generating and outputting a data signal (out of 701b-708b) from the first image signal and the second image signal, the gray scale voltage and the source driving control signal all of which are input from said signal processor;

a printed circuit board having a plurality of wires for transmitting the signals and/or voltages of said signal processor to the data signal driver (Fig. 6, col. 1, line 64-col. 2, line 12);

a gate signal driver for generating and outputting a gate signal from the gate voltage and the gate driving control signal of said signal processor (col. 2, lines 55-64);

a liquid crystal display panel (100) for displaying an image formed by receiving the data signal from said data signal driver and the gate signal from said gate signal driver (col. 2, lines 55-64);

wherein the plurality of wires comprises a first group of wires for transmitting the first image signal and a second group of wires for transmitting the second image signal (Fig. 3, a plurality of wires grouped on the left and on the right of G/A), and the first group of wires are

entirely spaced apart from the second group of wires (col. 1, line 64-col. 2, line 12, col. 3, lines 7-27));

wherein the data signal driver includes two groups of the data signal driver outputting a data signal from the first and the second image signal, one of which the left side of the signal processor and the other which is the right side of the processor (Fig. 3, col. 3, lines 7-27).

Kinoshita et al fail to disclose a gray scale voltage. Hashimoto discloses a matrix liquid crystal display including gray level voltage (Fig. 1, item 6) and a gray level voltage generator (16). It would have been obvious to incorporate the features of Hashimoto into that of Kinoshita et al as they both disclose LCD displays. The addition of the features of Hashimoto is advantageous as it consumes less power and is more efficient.

Kinoshita et al and Hashimoto fail to disclose where the first image signal and second image signal are simultaneously output. Ikeda et al discloses a driving circuit for a matrix type liquid crystal with two data drivers as shown in Figs. 1a, 16, 17b, items 105-1 and 105-2, where the signals are simultaneously output (col. 11, lines 11-45). It would have been obvious to one of ordinary skill in the art to incorporate the feature of two data drivers outputting simultaneous signals into Kinoshita et al as disclosed by Ikeda et al in col. 5, lines 31-40 where power consumption is reduced without deteriorating the operating efficiency of the liquid crystal display system.

As to independent claim 9, limitations of claim 1, and further comprising, wherein the data signal driver comprises at least four source drive integrated circuits and is physically, electrically connected to said liquid crystal display panel by a connecting member mounting the source drive integrated circuits one to one, wherein the connecting member includes a first group of connecting member and a second group connecting member, the first group of connecting

Art Unit: 2675

member being connected with the first group of wires and the second group connecting member being connected with the second group of wires (Fig. 3, col. 1, line 64-col. 2, line 28, col. 3, lines 7-27).

Kinoshita et al and Hashimoto fail to disclose where the first image signal and second image signal are simultaneously output. Ikeda et al discloses a driving circuit for a matrix type liquid crystal with two data drivers as shown in Figs. 1a, 16, 17b, items 105-1 and 105-2, where the signals are simultaneously output (col. 11, lines 11-45). It would have been obvious to one of ordinary skill in the art to incorporate the feature of two data drivers outputting simultaneous signals into Kinoshita et al as disclosed by Ikeda et al in col. 5, lines 31-40 where power consumption is reduced without deteriorating the operating efficiency of the liquid crystal display system.

As to dependent claim 2, see limitation of claim 9, above.

As to dependent claims 3 and 10, limitations of claims 2 and 9, and further comprising, wherein the first image signal includes a first clock signal (Fig. 3, item LCK-L) and the second image signal includes a second clock signal (Fig. 3, item LCK-R), and the first clock signal and the second clock signal have a frequency half of a clock signal frequency supplied from the image supplying source (col. 5, lines 3-50)

As to dependent claims 4 and 11, limitations of claims 2 and 9, and further comprising, wherein the first image signal includes a first shift signal and the second image signal includes a second shift signal, the first and second shift signals being respectively applied to a source drive integrated circuit of a corresponding group of the source drive integrated circuits such that the group of the source drive integrated circuits have the same phase (col. 4, lines 8-24).

Art Unit: 2675

As to dependent claim 5, limitations of claim 2, and further comprising, wherein the first image signal includes a first drive signal and the second image signal includes a second drive signal, the first and second drive signals being respectively applied to a source drive integrated circuit of a corresponding group of the source drive integrated circuits such that the group of the source drive integrated circuits have the same phase (col. 3, lines 7-27).

As to dependent claims 6 and 12, limitations of claims 2 and 9, and further comprising, wherein the first group of wires and the second group of wires are branched from a wire aggregation including a plurality of wires at a selected position (Figs. 3 and 4).

As to claims 7 and 8, see claim 1.

Response to Arguments

Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Srilakshmi K. Kumar whose telephone number is 703 306 5575. The examiner can normally be reached on 8:00 am to 4:30 pm.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, xxxx xxxx can be reached on xxx xxx xxxx. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2675

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Srilakshmi K. Kumar
Examiner
Art Unit 2675

SKK
October 20, 2004



DENNIS-DOON CHOW
PRIMARY EXAMINER